

micro and nanoelectronics
microsystem
ambient intelligence
image chain
biology and health



2008

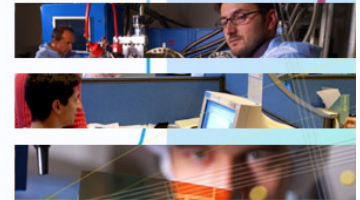
System Compilation for MPSoC based on NoC

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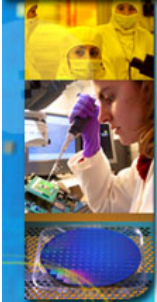
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Outline

- MPSoC Based on NoC
- NoC and Programming models
- System Compilation for NoC.



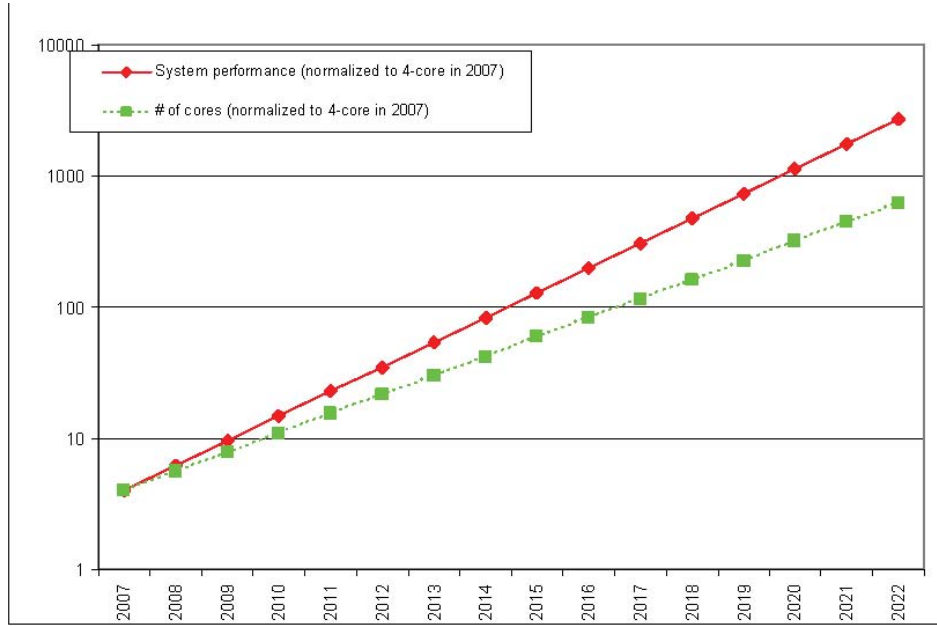
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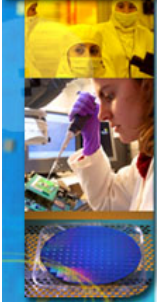


SOC Networking Driver Trends [ITRS]



4 Cores in 2007, 10 in 2010 and 100 in 2016

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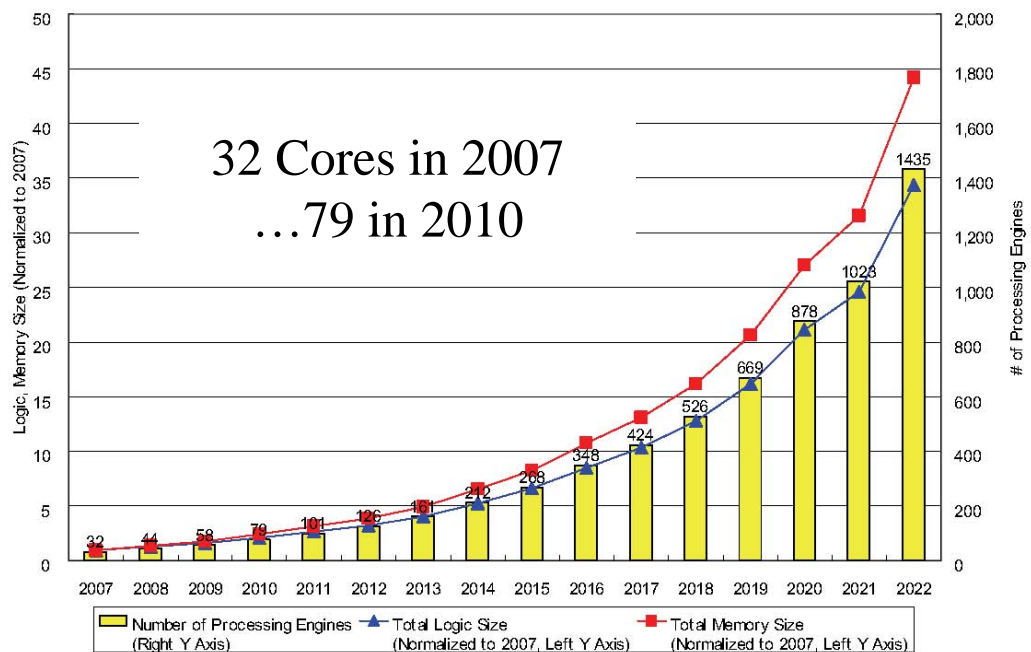
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SOC Consumer Portable Design Complexity Trends [ITRS]

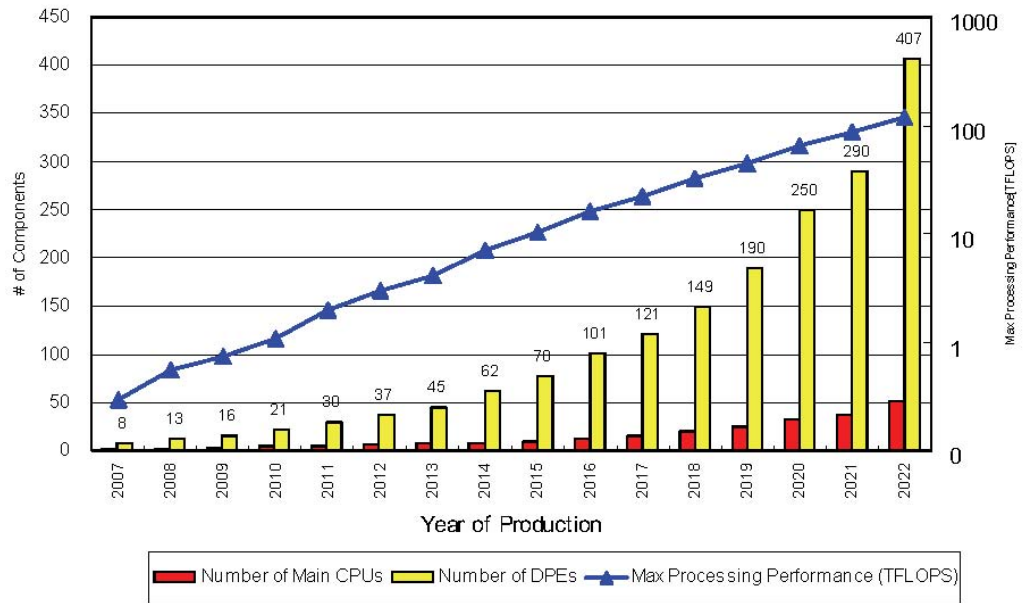


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SOC Consumer Stationary Design Complexity Trends [ITRS]

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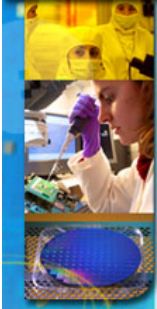


Correspondence Between System-Level Design Requirements and Solutions [ITRS]

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<i>Requirement</i>	<i>Solution</i>
<i>Design block reuse</i>	System-level component reuse On-chip network design methods
<i>Available platforms environments</i>	Multi-fabric implementation planning (AMS, RF, MEMS, ...)
<i>Platforms supported</i>	Automated interface synthesis Automated HW-SW co-design and -verification
<i>Accuracy of high level estimates</i>	Improved system-level power -estimation techniques Chip-package co-design methods
<i>SOC reconfigurability</i>	On-chip network design methods
<i>Analog automation</i>	Multi-fabric implementation planning (AMS, RF, MEMS, ...)
<i>Modeling methodology, description languages, simulation environments</i>	Mixed-Signal/RF verification

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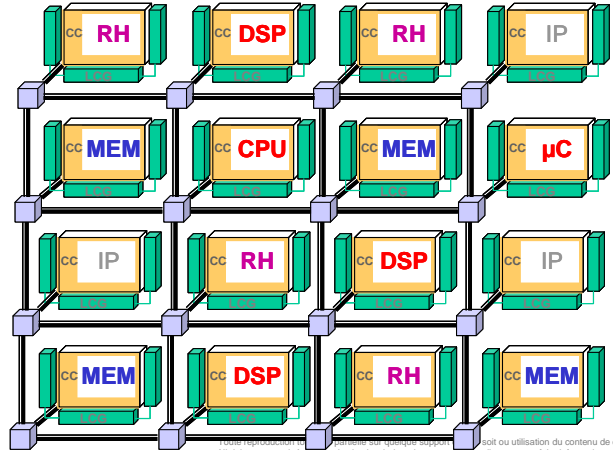
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What is an MPSoC based on NoC?

- “NoC is an interconnection structure for exchanging information on a chip between heterogeneous or homogeneous HW/SW resources”



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NoC Research world-wide

xPIPES, Stanford&Bologna Univ.

Best Effort NoC

- SPIDERGON, STM
- PROTEO, Tampere Univ.
- DSPIN, LIP6

NoC with QoS

- ETHERREAL, Philips
- FAUST, LETI

NoC on FPGA

- HERMES, PUCRS
- GECKO, IMEC

Asynchronous NoC

- CHAIN, UK

NoC start-up

- SILISTIX, UK
- ARTERIS, FR
- INOCS, CH

Industrial products

- TILERA, US
- PICOCHIP, US
- TERAFLOP, US
- Sonics, US

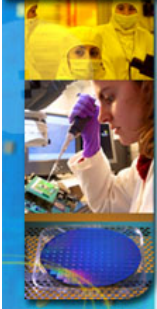
More than 60 projects

- Universities and Industries

Convergent Technique choices

- 2-D topology
- Deterministic routing
- Packet commutation

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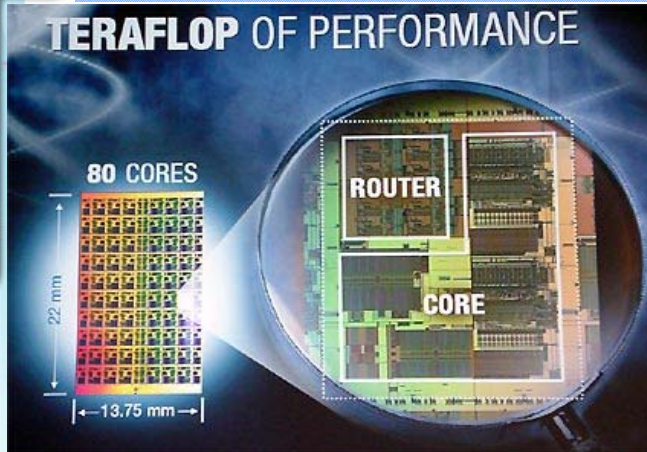
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Intel's TERAFL0P



80 floating-point cores
NoC packet switching
65nm
275 mm²
1.28TFLOPS
4GHz
98W

- An impressive realization...
- But : what about application mapping on such a platform ?

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NoC and programming model

- Programming model
 - “An abstract conceptual view of the structure and operation of a computing system”
 - A set of mechanisms (hardware and/or software) to help an **application** to map on an **underlying system**

⇒ A link between the application and the system

⇒ Fields of research: application description, programming languages, compilers, libraries, **communication systems, I/O**

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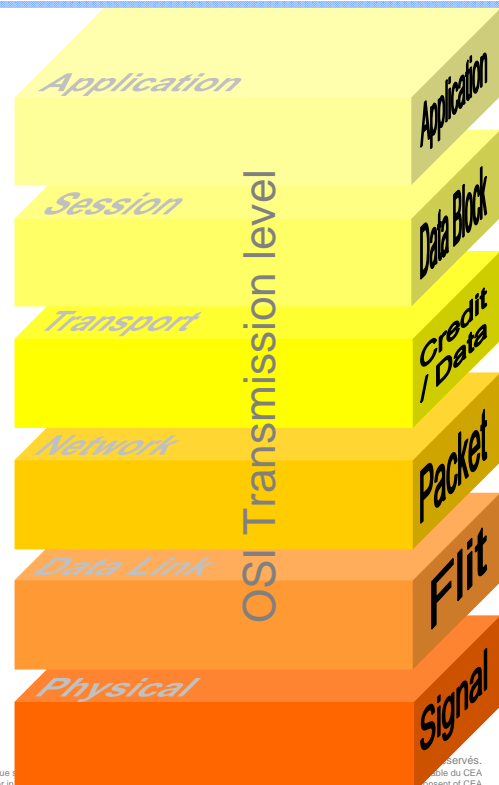
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Programming NoC = Configure Protocol Stack

Programming model of the NoC-based platform is essential. It can determine :

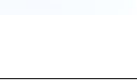
- Reconfiguration management
- Task synchronization
- Power management
- Bandwidth allocation
- End-to-end flow control
- Protocol wrappers
- Packet routing
- GALS strategy



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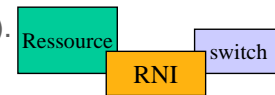
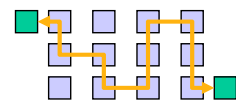
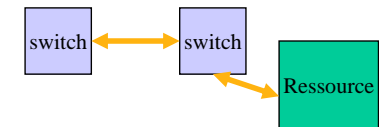
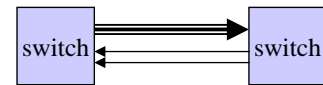
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SW code and Configuration Parameters for HW Layers



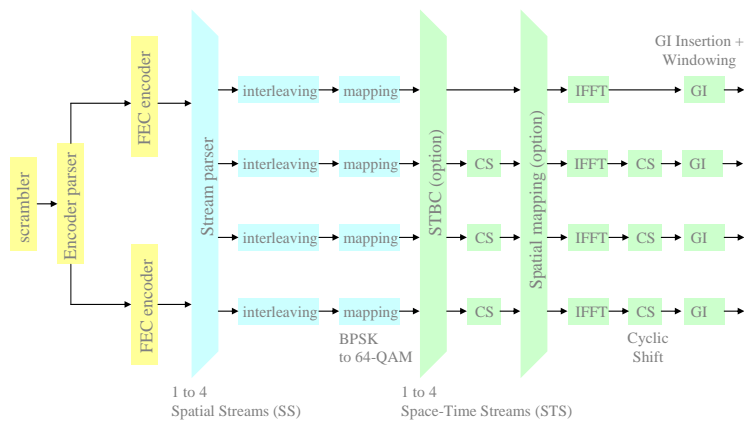
- SW Code is generated for the upper layers
- Configuration parameters are generated for the layers implemented in HW, generally the four lower layers of the OSI reference model

- Physical layer:** determines the number and length of wires connecting resources and switches. Unit of communication: electrical signal
- Data link layer:** defines a protocol to transmit information between entities (switch, resource). It may include flow control and error correction. Unit : bits and words
- Network layer:** defines how data are transmitted over the network from an sender to a receiver (routing algorithm) Unit : packet, flit
- Transport layer:** establishes and maintains end-to-end connections. Its performs packet segmentation and reassembly and ensure message ordering (Resource Network Interface). Unit : message



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Application complexity: 802.11n (wifi)



Example of 802.11n encoding stream

802.11n

144 communications modes

2 potential coding streams, 1 to 4 antennas

1 to 4 spatial streams 1 to 4 space-time streams

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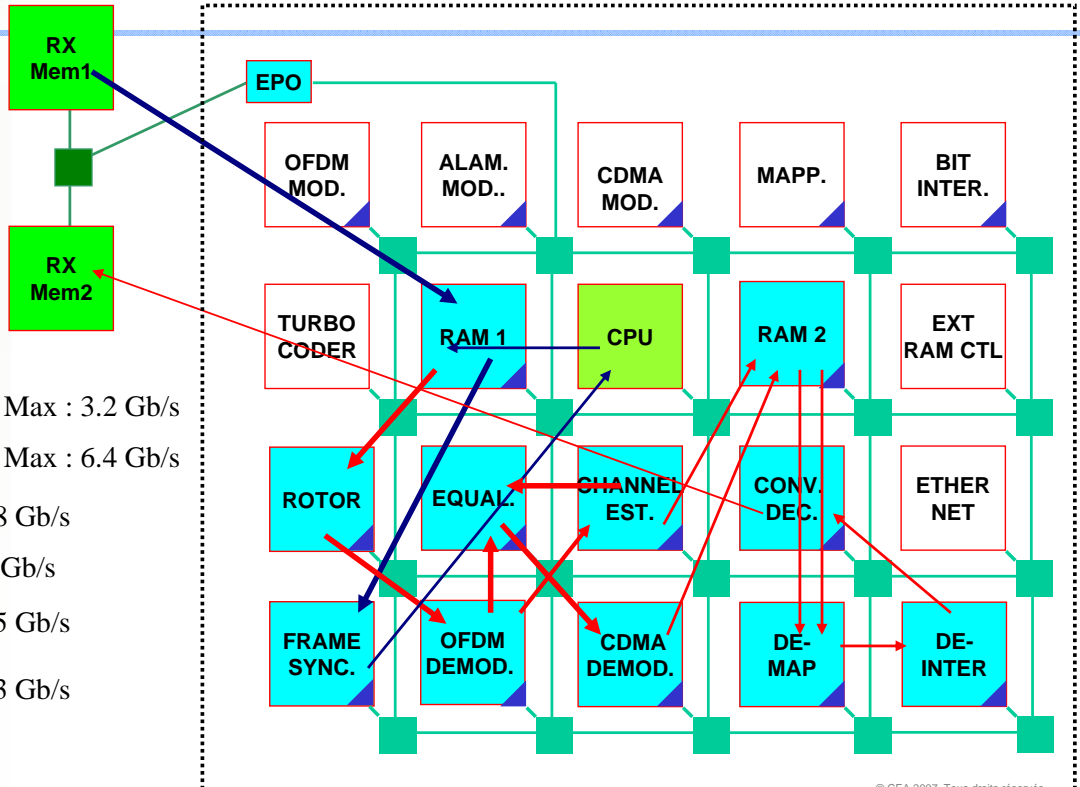
Application Example Traffic (RX)



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Th. Max : 3.2 Gb/s

Th. Max : 6.4 Gb/s

2.08 Gb/s

1.7 Gb/s

0.85 Gb/s

0.03 Gb/s

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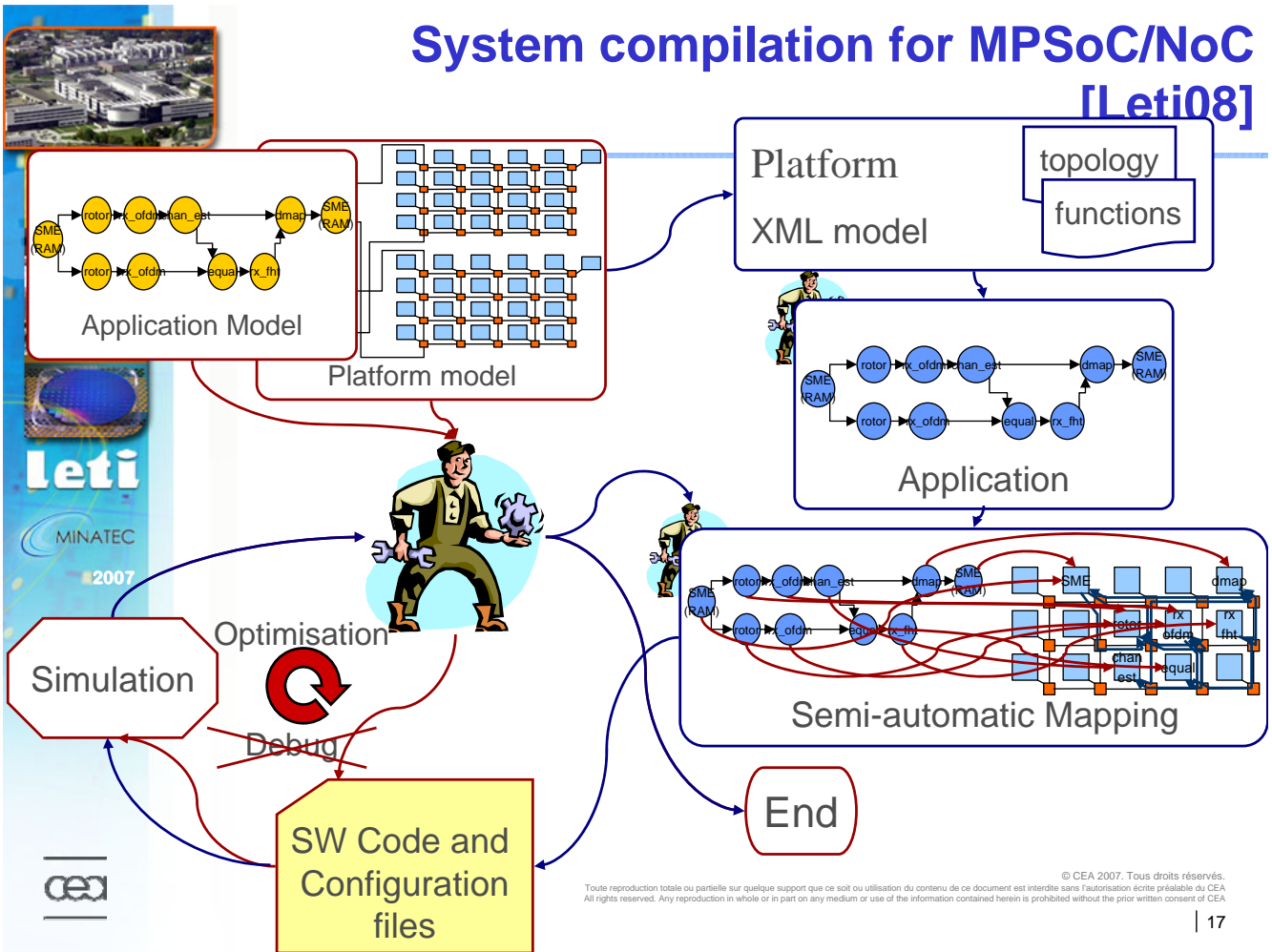


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System compilation for MPSoC/NoC [Leti08]



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Many thanks

■ LETI's team

- F. Clermidy, P. Vivet, E. Beigné, Y. Thonnart, R. Lemaire

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